**Annexure ‘CD – 01’**





**FORMAT FOR COURSE CURRICULUM**

**Course Title: Digital Electronics and Computer Organization Credit Units: 5**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **L** | **T** | **P/S** | **SW/FW** | **No. of PSDA** | **TOTAL CREDIT UNITS** |
| 3 | - | 2 | 2 | 3 | 5 |

**Course Level: UG Course Code: CSE207**

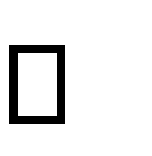
**Course Objectives:** This course covers combinational and sequential logic circuits. Course of digital electronics is the study of electronic circuits that are used to process and control digital signals.

**Pre-requisites: Software Engineering:** Students studying the “digital electronics” course must have basic knowledge of physics (electricity) which is the operational basis of most digital devices.

**Course Contents/Syllabus:**

|  |  |
| --- | --- |
|  | **Weightage (%)** |
| **Module I** Digital electronics | **25%** |
| Combinational Logic Modules and their applications, Decoders, encoders, multiplexers, de multiplexers and their applications; Parity circuits and comparators; Arithmetic modules- adders, subtractors and ALU, Register Transfer, Bus and Memory Transfers, Arithmetic Micro-operations, Logic Micro-operations, Shift Micro-operations, Arithmetic Logic  shift Unit. |
| Module II Basic Computer Organizations and Design | **20%** |
| Instruction Codes, Computer Registers, Computer Instructions, Timing and Control, Instruction Cycle, MemoryReference Instructions, Input-Output and Interrupt, Design of Accumulator Logic. Hardwired and Microprogrammed control:  Control Memory, Address Sequencing, Design of Control Unit |
| Module III Central Processing Unit | **20%** |

|  |  |
| --- | --- |
| Introduction, General Register Organization, Stack Organization, Instruction representation, Instruction Formats, Instruction type, Addressing Modes, Data Transfer and Manipulation, Program Control, Reduced Instruction Set Computer RISC and CISC Computer Arithmetic: Introduction, Multiplication Algorithms, Division Algorithms, Floating-Point Arithmetic Operations |  |
| Module IV Memory Organization | **20%** |
| **Memory Organization:** Memory Hierarchy, Main Memory**:** RAM and ROM Chips, Address Map, Memory Connection to CPU. Auxiliary Memory**:** Disks and Tapes. Associative Memory**:** Hardware Organization, Match Logic, Read. Operation and Write Operation. Cache Memory: Associative Mapping, Direct. Mapping, Set-Associative Mapping, Writing into Cache Initialization. Virtual Memory**:** Address and Memory Space, Address Mapping, Page Replacement.  Intersystem communication and I/O : Peripheral Devices, Input-Output Bus concept, Bus cycle, Synchronous and asynchronous transfer, Interrupt handling in PC. |  |
| Module V Pipelining, Vector Processing and Multiprocessors | **15%** |
| Parallel Processing, Pipelining, Arithmetic Pipeline, Instruction Pipeline, RISC Pipeline, Vector Processing, Array Processors.  Multiprocessors: Characteristics of Multiprocessors, Interconnection Structures,  Interprocessor Arbitration, Interprocessor Communication and Synchronization. |

**Course Learning Outcomes:**

1. Upon completion of the course students will be able to Demonstrate how gate functions are achieved.
2. Use Boolean algebra to define different logic operations.
3. Course will deliver that how counting, decoding, multiplexing and clocks are accomplished with logic devices.
4. Course will deliver that how arithmetic operations are achieved with digital circuitry
5. Course will deliver in depth study of pipelining and Multiprocessors
6. Course will the in depth study of memory organization and Intersystem communication
7. Design, implement and evaluate a computer based process, component or program to meet desired needs

**Pedagogy for Course Delivery:**

* Videos and power point presentations.
* Assignments and Tutorials for continuous assessment.
* Virtual lab/ orcad for lab
* class room teaching (face to face /remote teaching using e-content )

**List of Professional Skill Development Activities (PSDA):**

* 1. **Case Study**
  2. **Quiz**
  3. **Minor Experiment**

**Lab/ Practicals details, if applicable:**

**List of Experiments:**

1. Simulation using ORCAD
2. To simulate Half Adder circuit
3. To simulate Full Adder Circuit
4. To simulate the logical part of a simple Arithmetic logical Unit **5.** To simulate a 4-bit binary adder-subtractor circuit
5. Simulation of one digit BCD Adder.
6. To simulate and study the tristate buffer
7. To simulate the common bus using tri-state buffers and decoder
8. To simulate the common bus using multiplexers.
9. Study of 8085 Microprocessor
10. Study of instruction set of 8085 microprocessor Open Ended program: Designing of various type parser

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**Assessment/ Examination Scheme:**

|  |  |
| --- | --- |
| **Theory L/T (%)** | **Lab/Practical/Studio (%)** |
| **80** | **20** |

**B.Tech Theory Assessment (L&T):**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
|  | **Continuous Assessment/Internal Assessment 40%** | | | | | | **End Term Examination 60%** |
| **Components (Drop down)** | Attendance | Class Test | Assignment | Viva | Group  Presentation | Quiz | **EE** |
| Linkage of PSDA with Internal Assessment Component, if any |  |  |  | 3 | 3 | 10 |  |
| **Weightage (%)** | 5 | 15 | 4 |  |  |  | 60 |

**Lab/ Practical/ Studio Assessment:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Continuous Assessment/Internal Assessment 40%** | | | | | **End Term Examination 60%** | |
| Components (Drop down | Performance | Lab Record | Viva | Attendance | Practical | viva |
| Weightage (%) | 15 | 10 | 10 | **5** | **30** | **30** |

**Text Reading:**

1. Morris Mano, Computer System Architecture, 3rd Edition – 1999, Prentice-Hall of India Private Limited.
2. Harry & Jordan, Computer Systems Design & Architecture, Edition 2000, Addison Wesley, Delhi

**References:**

1. *WIliam Stallings, Computer Organization and Architecture, 4th Edition-2000, Prentice-Hall of India Private Limited.*
2. *Kai Hwang-McGraw-Hill, Advanced Computer Architecture.*